CLAIMS

Please amend the claims as follows:

1.-11. (canceled)

12. (currently amended) A method of reporting simulation data obtained by the simulation of an electronic design within a data processing system, said method comprising:

a simulator running a testcase against a simulation model of the electronic design, wherein:

the simulation model is formed of representations of instances of a plurality of design entities,

the instances of the design entities contain a plurality of signals and functional logic that define functional operation of the electronic design,

each instance of at least a particular design entity of the plurality of design entities contains an instance of an instrumentation entity that monitors the containing instance of the particular design entity but does not contribute to functional operation of the electronic design, and

each instance of the instrumentation entity contains a trace array logically coupled to receive a monitored signal set including at least one signal among the plurality of signals, wherein the trace array is further logically coupled to receive a control signal among the plurality of signals;

recording trace data for the monitored signal set within the trace array during the running of the testcase, wherein the recording includes concurrently storing within the trace array multiple values of the monitored signal set obtained over multiple cycles of functional operation of the simulation model, wherein recording trace data includes:

recording, within the trace array, values assumed by the monitored signal set during only those cycles of functional operation during which the control signal is asserted and refraining from recording values assumed by the monitored signal set during those cycles of functional operation during which the control signal is not asserted, such

that no values assumed by the monitored signal set are recorded for those cycles of functional operation during which the control signal is not asserted; and

recording within the trace array a number of functional cycles elapsed between said values assumed by the monitored signal set;

exporting said trace data from said trace array in a trace file and storing said trace file in data storage.

13.-26. (canceled)

27. (currently amended) A data processing system, comprising:

means for running a testcase against a simulation model of an electronic design, wherein:

the simulation model is formed of representations of instances of a plurality of design entities,

the instances of the design entities contain a plurality of signals and functional logic that define functional operation of the electronic design,

each instance of at least a particular design entity of the plurality of design entities contains an instance of an instrumentation entity that monitors the containing instance of the particular design entity but does not contribute to functional operation of the electronic design, and

each instance of the instrumentation entity contains a trace array logically coupled to receive a monitored signal set including at least one signal among the plurality of signals, wherein the trace array is further logically coupled to receive a control signal among the plurality of signals;

means for recording trace data for the monitored signal set within the trace array during the running of the testcase, wherein the recording includes concurrently storing within the trace array multiple values of the monitored signal set obtained over multiple cycles of functional operation of the simulation model, wherein the means for recording trace data includes:

means for recording, within the trace array, values assumed by the monitored signal set during only those cycles of functional operation during which the control signal is asserted and for refraining from recording values assumed by the monitored signal set during those cycles of functional operation during which the control signal is not

asserted, such that no values assumed by the monitored signal set are recorded for those cycles of functional operation during which the control signal is not asserted;

means for recording in the trace array a number of functional cycles elapsed between said values assumed by the monitored signal set; and

means for exporting said trace data from said trace array in a trace file and storing said trace file in data storage.

28.-41. (canceled)

42. (currently amended) An apparatus comprising:

a computer usable medium containing program code, said program code including:

instructions for running a testcase against a simulation model of an electronic design, wherein:

the simulation model is formed of representations of instances of a plurality of design entities,

the instances of the design entities contain a plurality of signals and functional logic that define functional operation of the electronic design,

each instance of at least a particular design entity of the plurality of design entities contains an instance of an instrumentation entity that monitors the containing instance of the particular design entity but does not contribute to functional operation of the electronic design, and

each instance of the instrumentation entity contains a trace array logically coupled to receive a monitored signal set including at least one signal among the plurality of signals, wherein the trace array is further logically coupled to receive a control signal among the plurality of signals; and

instructions for recording trace data for the monitored signal set within the trace array during the running of the testcase, wherein the recording includes concurrently storing within the trace array multiple values of the monitored signal set obtained over multiple cycles of functional operation of the simulation model, wherein the instructions for recording trace data include[[s]]:

instructions for recording, within the trace array, values assumed by the monitored signal set during only those cycles of functional operation during which the control signal is asserted and for refraining from recording values assumed by the monitored signal set during those cycles of functional operation during which the control signal is not asserted, such that no values assumed by the monitored signal set are recorded for those cycles of functional operation during which the control signal is not asserted;

instructions for recording in the trace array a number of functional cycles elapsed between said values assumed by the monitored signal set; and

instructions for exporting said trace data from said trace array in a trace file and storing said trace file in data storage.

43.-51. (canceled)

52. (previously presented) The method of Claim 12, wherein exporting the trace data in a trace file includes exporting the trace data in a trace file indicating an association between a value of said monitored signal set and an enumerated value containing a textual string.

53. (canceled)

54. (currently amended) The method of Claim [[53]] 12, wherein:

the trace array has a counter that counts the functional cycles; and

said recording trace data includes recording in the trace array an entry indicating overflow of said counter.

55. (currently amended) The method of Claim 12, and further comprising:

during functional operation, the instrumentation entity signaling that the trace array is full;

in response to said signaling, automatically halting running of the testcase prior to completion of the testcase and performing said exporting; and

thereafter, resuming running of the testcase.

56. (previously presented) The method of Claim 12, wherein said exporting includes:

exporting a trace file including a plurality of fields, said plurality of fields including at least one of a set comprising a file version field and an array type field indicating one of plurality of trace array types.

57. (previously presented) The method of Claim 12, wherein said storing comprises:

for each of a plurality of simulation runs, grouping all trace files from that simulation run in a respective one of a plurality of file system subdirectories that are each dedicated to one of the plurality of simulation runs.

58. (previously presented) The method of Claim 12, wherein said storing comprises automatically naming the trace file in data storage by a filename indicating the containing instance of the particular design entity.

59. (previously presented) The method of Claim 12, and further comprising accessing the trace file in data storage with a trace analysis tool.

60.-65. (canceled)

66. (previously presented) The data processing system of Claim 27, wherein said means for exporting the trace data in a trace file includes means for exporting the trace data in a trace file indicating an association between a value of said monitored signal set and an enumerated value containing a textual string.

67. (canceled)

68. (currently amended) The data processing system of Claim 27 [[67]], wherein:

the trace array has a counter that counts the functional cycles; and

said means for recording trace data includes means for recording in the trace array an entry indicating overflow of said counter.

69. (currently amended) The data processing system of Claim 27, and further comprising:

means for detecting signaling by the instrumentation entity during functional operation that the trace array is full;

means, responsive to said signaling, for automatically halting running of the testcase prior to completion of the testcase; and

means for resuming running of the testcase after exporting said trace data.

70. (previously presented) The data processing system of Claim 27, wherein said means for exporting includes:

means for exporting a trace file including a plurality of fields, said plurality of fields including at least one of a set comprising a file version field and an array type field indicating one of plurality of trace array types.

71. (previously presented) The data processing system of Claim 27, wherein said means for storing comprises:

means, for each of a plurality of simulation runs, for grouping all trace files from that simulation run in a respective one of a plurality of file system subdirectories that are each dedicated to one of the plurality of simulation runs.

72. (previously presented) The data processing system of Claim 27, wherein said means for storing comprises means for automatically naming the trace file in data storage by a filename indicating the containing instance of the particular design entity.

73. (previously presented) The data processing system of Claim 27, and further comprising a trace analysis tool for accessing the trace file in data storage.

74.-79. (canceled)

80. (previously presented) The apparatus of Claim 42, wherein the instructions for exporting the trace data in a trace file include instructions for exporting the trace data in a trace file indicating

an association between a value of said monitored signal set and an enumerated value containing a textual string.

81. (canceled)

82. (currently amended) The apparatus of Claim 42 [[81]], wherein:

the trace array has a counter that counts the functional cycles; and

said instructions for recording trace data include instructions for recording in the trace array an entry indicating overflow of said counter.

83. (currently amended) The apparatus of Claim 42, and further comprising:

instructions for detecting signaling during functional operation by the instruction entity that the trace array is full;

instructions, in response to said signaling, for automatically halting running of the testcase prior to completion of the testcase and performing said exporting; and

thereafter, resuming running of the testcase.

84. (previously presented) The apparatus of Claim 42, wherein said instructions for exporting include:

instructions for exporting a trace file including a plurality of fields, said plurality of fields including at least one of a set comprising a file version field and an array type field indicating one of plurality of trace array types.

85. (previously presented) The apparatus of Claim 42, wherein said instructions for storing comprise:

instructions that, for each of a plurality of simulation runs, group all trace files from that simulation run in a respective one of a plurality of file system subdirectories that are each dedicated to one of the plurality of simulation runs.

86. (previously presented) The apparatus of Claim 42, wherein said instructions for storing comprises instructions for automatically naming the trace file in data storage by a filename indicating the containing instance of the particular design entity.

87. (previously presented) The apparatus of Claim 42, and further comprising a trace analysis tool for accessing the trace file in data storage.